

ABSTRACT OF THE DISCLOSURE

A circuit for testing a chip. The chip has an intellectual product circuit module, and the circuit has a multiplexer controller, several registers and a MUX finite state machine controller to configure these registers in different states according to the test patterns. In
5 the next state, a test activating signal is provided to the intellectual product circuit module. The intellectual product circuit module is then operated and tested according to the output of the registers.

10039852.102201
T0220T.2586E00T